AMENDMENTS TO THE CLAIMS:

Please amend claims 27, 28, and 31-33, as indicated below.

This listing of claims will replace all prior versions and listings of claims in the application:

1. - 26. (Canceled)

27. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including a first and second region separated by an isolation element;

a first transistor formed on [[a]] the first region of the substrate and including a first insulation film and a first gate electrode arranged along a first direction; and

a second transistor formed on [[a]] the second region of the substrate and including a second insulation film and a second gate electrode arranged along the first direction,

wherein a side wall of the [[said]] first gate electrode ~~at one end of a channel direction~~ is connected to a side wall of the [[said]] second gate electrode ~~at one end of the channel direction~~ above the isolation element when viewed from a direction perpendicular to the first direction.

28. (Currently Amended) A device according to claim [[27]] 33, wherein ~~a part of the side wall of the first gate electrode is only connected to a part of the side wall of the second gate electrode and said part of the side wall of the first gate electrode and said part of the side wall of the second gate electrode are~~ the side insulator film is substantially perpendicular to a surface of said semiconductor substrate.

29. (Canceled)

30. (Previously Presented) A device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.

31. (Currently Amended) A device according to claim [[27]] 33, wherein ~~said first transistor includes a first insulator film, said second transistor includes a second insulator film,~~ said first ~~insulator~~ insulation film is thinner than said second ~~insulator~~ insulation film, said first transistor ~~is included in~~ forms a logic circuit, and said second transistor ~~is included in~~ forms a memory cell.

32. (Currently Amended) A device according to claim [[27]] 33, wherein top surfaces of said first and second gate electrodes ~~and a connection layer~~ are coplanar.

33. (Currently Amended) A device according to claim 27, wherein said second transistor further comprises ~~a gate insulator film formed on the substrate,~~ a polysilicon layer formed on the second insulation film formed on the substrate ~~gate insulator film~~, and a side insulator film formed on a side wall of the ~~gate insulator~~ second insulation film and a side wall of the polysilicon layer, said second gate electrode is formed on the polysilicon layer, ~~and said~~ the side wall of said first gate electrode is directly connected to [[the]] a side wall of said second gate electrode and ~~a side wall of said side insulator film~~ connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film.